REMARKS/ARGUMENTS

The Examiner is thanked for granting an interview on September 25, 2005. As was respectfully submitted during the interview, it is noted that U.S. Patent No. 6,075,942 (*Cartwright, Jr.*) states that:

> A first computer system (34) compiles a source program into machine code for a register-oriented microprocessor, optimizing the global allocation of microprocessor registers in the process. It then translates the resultant code into generic-machine operand-stack-oriented code. In performing the translation, it generates code that preserves the register-oriented code's microprocessor-register allocation by filling the operand stack from local variables chosen in accordance with a predetermined correspondence between local variables and microprocessor registers. That code also stores the operand stack's contents in accordance with that same correspondence. A second computer system (32), which employs the register-oriented microprocessor, converts the resultant generic machine code into its own machine code in accordance with the same association between local variables to microprocessor registers. (Abstract)

In the Office Action, the Examiner has asserted that Col. 12, lines 25-30 and 35-40 of (*Cartwright, Jr.*) teaches a reduced-set of virtual machine instructions that includes a first plurality of virtual machine instructions that collectively represent a complete set of virtual machine instruction which can be used to implement a virtual machine, wherein the number of virtual machine instructions of the reduced-set is less than the number of instructions in a larger-set that collectively represent a complete set of instructions.

The section of (*Cartwright, Jr.*) which is the basis of the rejection is reproduced below for the Examiner's convenience:

> In place of the eighth row's table of ordinarily formatted code attributes, some embodiments may use a table of a different attribute type, one whose contents include, say, a data-reduced ("compacted") version of the warped code. In that case the virtual machine would have to re-expand the contents before using them.
>
> Some implementations of the present invention's broader teachings may not constrain global register allocation as much as the previously described embodiments do. FIG. 10 illustrates such an implementation. FIG. 10's parsing-and-analysis and machine-independent-optimization steps 66 and 68 are similar to corresponding steps of FIGS. 4 and 8, but FIG. 10 employs a step 70 that generates code for, say, a generic register-oriented machine of the reduced-instruction-set-computing ("RISC") class. In other words, it would generate code not for the generally recognized stack-oriented virtual machine but rather for a virtual machine that implements specific, register-oriented instructions. The assumed architecture would not necessarily match that of any real-world microprocessor, and it might include an unlimited, or very large, number of registers, i.e., more registers than the typical real-world microprocessor. It is the resultant, generic RISC code whose

translation by the programmer's compiler into the stack-oriented virtual-machine code block 72 represents.

It is noted that the cited section which is the basis of the Examiner's rejection makes reference to a reduced-instruction-set-computing "RISC" class associated with a generic register-originated machine. However, it is respectfully submitted that the Examiner's rejection is improper because it does NOT specifically point out how or why a "RISC" instruction set teaches the claimed features of: a reduced virtual machine instruction set that represents a complete set of virtual machine instruction that can be used to implement a virtual machine, wherein the number of instructions is less than the number of a larger set of virtual machine instructions (e.g., conventional Java virtual machine instructions).

Based on the foregoing, it is submitted that all pending claims are patentably distinct over the cited art of record. Additional limitations recited in the independent claims or the dependent claims are not further discussed because the limitations discussed above are sufficient to distinguish the claimed invention from the cited art. Accordingly, Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Amendment is to be charged to Deposit Account No. 500388 (Order No. SUN1P811). Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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